# Código VHDL

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity sum\_res\_4bits is

Port ( A, B : in STD\_LOGIC\_VECTOR (3 downto 0);

C : inout STD\_LOGIC\_VECTOR (4 downto 0);

Cin : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (3 downto 0)

);

end sum\_res\_4bits;

architecture Behavioral of sum\_res\_4bits is

signal SEL : STD\_LOGIC\_VECTOR (3 downto 0);

begin

process (A, B, C, SEL)

begin

C(0) <= Cin;

for j in 0 to 3 loop

SEL(j) <= B(j) xor C(0);

S(j) <= A(j) xor SEL(j) xor C(j);

C(j+1) <= (A(j) and C(j)) or (A(j) and SEL(j)) or (SEL(j) and C(j));

end loop;

end process;

end Behavioral;

# Código del TEST-BENCH

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity t\_sum\_res\_4bits is

-- Port ( );

end t\_sum\_res\_4bits;

architecture Behavioral of t\_sum\_res\_4bits is

component sum\_res\_4bits is

Port ( A, B : in STD\_LOGIC\_VECTOR (3 downto 0);

C : inout STD\_LOGIC\_VECTOR (4 downto 0);

Cin : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (3 downto 0)

);

end component;

signal A, B, S : STD\_LOGIC\_VECTOR (3 downto 0);

signal Cin : STD\_LOGIC;

signal C : STD\_LOGIC\_VECTOR (4 downto 0);

begin

element : sum\_res\_4bits port map (

A => A,

B => B,

C => C,

Cin => Cin,

S => S

);

process

begin

--Caso 1: 6 + 7

A <= "0110";

B <= "0111";

Cin <= '0';

wait for 50 ns;

--Caso 2: 6 + 9

B <= "1001";

wait for 50 ns;

--Caso 3: 4 + 9

A <= "0100";

wait for 50 ns;

--Caso 4: 15 - 1

A <= "1111";

B <= "0001";

Cin <= '1';

wait for 50 ns;

--Caso 5: 3 + 10

A <= "0011";

B <= "1010";

Cin <= '0';

wait for 50 ns;

--Caso 6: 12 - 5

A <= "1100";

B <= "0101";

Cin <= '1';

wait for 50 ns;

--Caso 7: 14 - 8

A <= "1110";

B <= "1000";

wait for 50 ns;

--Caso 8: 10 - 6

A <= "1010";

B <= "0110";

wait for 50 ns;

--Caso 9: 9 - 4

A <= "1001";

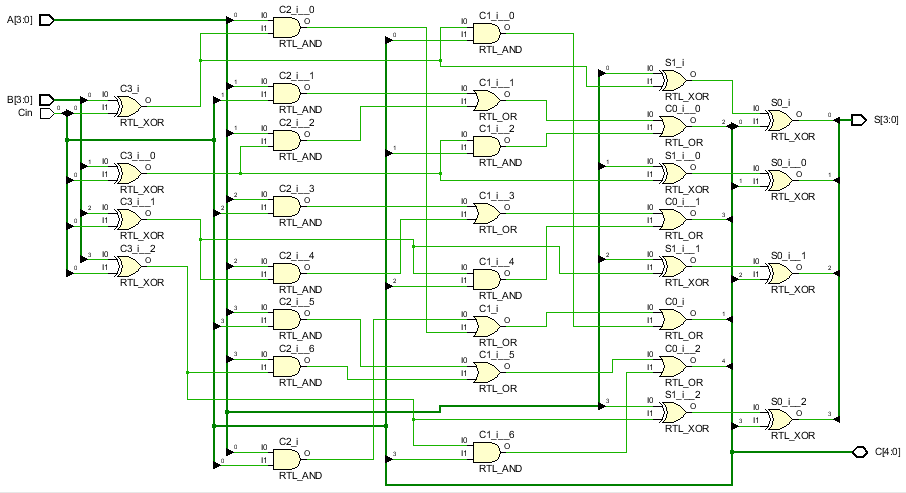
B <= "0100";

wait;

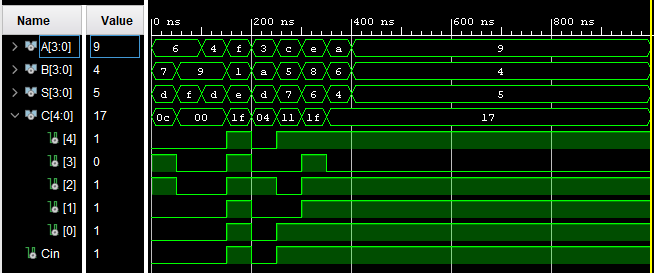
end process;

end Behavioral;

# Diagrama RTL



# Tabla de Resultados



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Operación | A | B | S | Cout |
| Suma | 6 | 7 | 13 | 0 |
| Suma | 6 | 9 | 15 | 0 |
| Suma | 4 | 9 | 13 | 0 |
| Resta | 15 | 1 | 14 | 1 |
| Suma | 3 | 10 | 13 | 0 |
| Resta | 12 | 5 | 7 | 1 |
| Resta | 14 | 8 | 6 | 1 |
| Resta | 10 | 6 | 4 | 1 |
| Resta | 9 | 4 | 5 | 1 |